4250 Series

Advanced Manufacturing Test Systems

The NEW flagship advanced manufacturing test system that offers a wide ranging capability in a compact package

- ***Maximum of 2048 test pins***
- ***NEW Non-Multiplexed Test Pin Card***
- ***Small Footprint***
- ***Single Box Solution***
- ***Windows 2000™ operating system***
- ***Automatic program generation software***
- ***Graphical program debug capability***
- ***Auto-debug facility***
- ***Inductive and capacitive vectorless test***
- ***Capacitor polarity testing***
- ***ISP and FLASH programming***
- ***Test program migration tools for Agilent and GenRad***

Building on the success of the original 4200 series, the 4250 is the new flagship of the IFR range of automatic test equipment. The smaller "footprint" of the 4250 requires some 33% less floorspace than the 4210/20 and as the 4250 contains an integrated PC based controller and all UUT power supplies, there is no need for any external computer or power supply cabinets. The operator interface is via an LCD monitor with optional touch screen. Full program and fixture compatibility is maintained with existing 4200 series test systems to ensure an easy transfer of programs. An optional migration package allows the reuse of your existing Agilent™ and GenRad™ test fixtures via a fixture adapter.

System Architecture

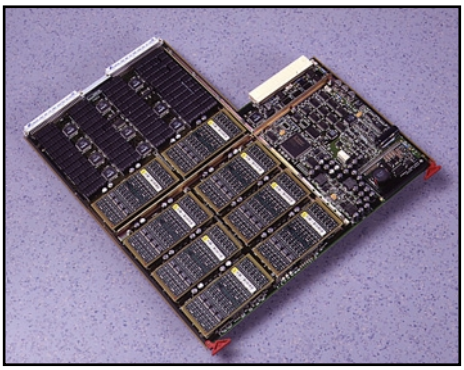
The 4250 series is controlled by an integrated industry standard PC running the Microsoft Windows 2000™ operating system. The system's graphical user interface has been designed to provide a familiar environment allowing new users to quickly progress along the learning curve.

Within the range, there are two models: the 4250 inclined interface (60°) and the 4250 horizontal interface.

Both models share a common card cage architecture and can be fitted with a range of cards selected from the list below to provide the most appropriate configuration:

- *Multiplexed Universal In-Circuit card - Provides high performance features such as negative drive voltages for ECL testing. Digital pins are multiplexed by a low ratio of 4:1.*
- *Non-Multiplexed Universal In-Circuit card - A new non-multiplexed card that provides a wide range of features, without placing limitations on test point allocation and fixture wiring. By using this card in preference to the multiplexed card, up to four times as many digital test pins may be used within a single device test, ideal for today's large ASIC's and CPLD's. Can be used in conjunction with the Multiplexed Card.*
- *Analog In-Circuit card - This cost-effective card provides analog only test pins suitable for MDA and pre-screening application. Q-test II Vectorless tests may be used in conjunction with this card enabling the correct soldering of digital devices to be verified.*
- *General Purpose Input/Output card - This option allows the user to add extra hardware facilities to the standard system, further extending its capabilities. Also used to control the Q-test II Vectorless test hardware.*
- *Instrument Access card - May be used to provide a high quality analog signal path (DC to 80 MHz) to the test fixture for use with external GPIB controlled instruments.*

- *Analog Functional Card - Includes a 4-channel arbitrary waveform generator and a two channel digital sampler. These can be used together with the graphical software tools to make a variety of analog functional tests.*



Non-Multiplexed Test Point Card

Analog and Digital Testing

The key to low test times is the optimization of analog tests, including contact, shorts and opens. The 4250 series offers a combination of high speed and exceptional accuracy through innovative pipeline and parallel processing techniques. A further factor is the utilization of advanced DSP measurements.

High guarding ratios and multi-wire measurements ensure component isolation and accurate diagnostics during In-Circuit tests. The ability to change all parameters associated with a measurement is vital to achieving the highest possible accuracy.

For mixed signal testing, such as ADC, DAC and CODEC devices, the 4250 series fully integrates its analog and digital capability. Every pin is backed by analog and digital resources and their ability to be used in conjunction with each other is a vital element in testing this important category of devices.

Every pin is provided with terminators to enable the testing of tri-state buses and open collector devices. Slew-rate controlled pin drivers ensure that vectors delivered to the testpoint are high integrity and load tolerant. Where necessary, full backdriving protection is provided.

For the testing of free running devices, 50 MHz clock synchronization and phase locking is provided. Vector rates of 5 MHz with 20 ns edge placement ensure that dynamic devices maintain keep-alive speed. Testing the most complex VLSI devices requires a range of advanced features such as hardware triggers, pin formatting and variable timing sets. On-the-fly jumps allow for program flow decisions to be made not only within the test program but also in real-time within an individual digital test.

The effectiveness of the 4250 series is further enhanced by the ability to program devices such as FLASH memory and CPLD's from manufacturers such as Xilinx™, Lattice™ and Altera™. This negates the need to invest in further equipment, adding extra value to the In-Circuit stage of the process.

Test Language

The MTL test language provided with the 4250 series provides the user with a high-level structured programming environment with fully integrated edit and debug facilities. The structure offers the twin benefits of top-level simplicity while also allowing the control of all system parameters at a lower level.

Simple language statements specify 'packaged' tests for common measurement types, selecting the most appropriate stimulus settings and measurement ranges automatically, reflecting the circuit configuration. These default settings can be altered by adding modifiers to the standard command through a simple graphical debug panel.

Although a compiled language, full interactive edit and debug is achieved through a high-speed incremental compilation process. The overall effect is the speed and power of a compiled language combined with the interactive nature of an interpreted language.

The graphical user interface features a menu system providing control of input/output and peripherals such as barcode readers and printers. Numeric data can be expressed in decimal, hexadecimal, octal and binary. Electrical engineering notation (e.g. 10 mV) is also fully supported for application orientated manipulation of test parameters and results.

Test Program Generation

Test programs are normally generated from the CAD data used to describe the board under test. The IFR FABmaster package is used to link to a wide range of CAD formats, producing a .CB format circuit description file and enabling fixture customization. The .CB file is then used to create a program using the IFR CAPG (Computer Assisted Program Generation) package.

This approach ensures that time-to-market is maintained by quick and accurate creation of fixture and program data. In order to reduce the subsequent debug time, CAPG uses an analog circuit simulator to predict the effectiveness of any guard pins that it adds to the test program.

All of the test methods supported by the 4250 series are fully integrated into CAPG. The interface is designed to allow the test engineer the maximum flexibility in using the most appropriate test for each device present on the board.

Graphical Debug Tools

A suite of debug tools is used to quickly commission the test program and fixture, again reducing the time-to-market aspects to the test process. In the case of analog measurements, a histogram display is used to dynamically display results with reference to nominal values and tolerances. Digital tests show state and timing information across the whole of the pinface in use during a particular test. Flow trace and test structure diagrams are also provided, fully integrated into the test editors. Each tool within the graphical debug suite gives point and click access to the whole range of parameters applicable to the test.

Auto-debug

This facility is designed to improve time-to-market by using automatic debug algorithms, independent of the programmer. By altering the range of measurement parameters and analyzing the subsequent results across a number of reiteration modes, the auto-debug facility is able to quickly commission a high proportion of analog In-Circuit tests. The graphical user interface allows user selection of all parameters to ensure the best results in the time available. Essentially, the auto-debug facility mimics the actions of a human programmer without the programmer being present.

Boundary Scan

The 4250 series fully supports the IEEE 1149.1 boundary scan standard for overcoming access and testability limitations. Automatic test generation is provided for boundary scan devices appearing singly or within scan paths. For boards with a scan path consisting of several devices, the 4250 Boundary Scan option can perform interconnect testing for both scan to scan nets and scan nets to physical test pins. These tests are derived from the CAD data describing the board and the BSDL (Boundary Scan Description Language) file pertaining to each device. The process is automatic and fully integrated into the IFR CAPG facility with full manual override available to the programmer if required.

Functional Analog Testing

The cluster test facility is used to define and test the functionality of a number of components as a single logical entity. For instance, the individual components of an amplifier circuit could be tested individually using the In-Circuit capability, followed by a test to ensure that the full amplifier circuit is performing correctly.

Usually, the requirement to perform a cluster test is stimulated by one of two circumstances. First, cluster testing is a useful method of overcoming test access, allowing test to be performed from the access points provided. Alternatively, the throughput capability of the 4250 series often leaves extra time within the beat rate that can be utilized by performing the functional tests that would otherwise necessitate further test system investment.

Analog Functional Card

The optional Analog Functional Card (AFC) provides a 4 channel arbitrary waveform generator and a 2 channel 40 MHz digital sampler. The AFC occupies a single slot in the systems test point rack and can be connected to the UUT through the analog bus, direct into the test fixture or via high quality coaxial connections. A suite of visual software tools are provided allowing easy generation and commissioning of test programs using the AFC card.

Third-Party Fixture & Program Compatibility

By using the optional program migration software and an appropriate fixture adapter, the 4250 series can be used to transfer production test from a third-party competitive test system. This provides a cost-effective way of replacing older equipment, avoiding high upgrade and maintenance costs. Migration options are available for Marconi Instruments System 80 / Midata 500 series and various systems from Hewlett Packard, Agilent, GenRad and Philips.

For example, the migration method may retain the existing test fixture while CAPG is used to create a new MTL test program. This program will be based on wiring/connectivity data and (where possible) library models that have been extracted from the original program code.

Fixturing

In order to offer the maximum flexibility and reliability, the 4250 series uses the full range of IFR vacuum and pneumatic fixtures. Where necessary, more esoteric applications can be accommodated using the customized fixture capability of IFR's Production Test Services facility.

In addition to IFR's fixturing capability, a wide range of third party suppliers also offer fixtures for the 4250 series.

Vectorless Testing

IFR is unique in offering both inductive and capacitive vectorless techniques, ensuring wide test coverage across a range of components from complex ASICs to connectors. Inductive probing is performed using the IFR patented Q-test II technique, whilst capacitive tests use the industry standard Agilent TestJet™ probe. The presence of two alternatives for vectorless testing allows the test engineer to use the most appropriate for a given application, essentially matching the pros and cons of each technique to the devices under test. These two techniques contribute to the system's ability to generate tests for devices quickly and to accurately diagnose faults to enhance productivity and quality.

Capacitor Polarity

Although competitive methods have claimed the ability to test reversed capacitors, the IFR Capacitor Orientation Defect Analysis (CODA) technique offers a first with truly reliable and repeatable measurements. Both single components and those found with parallel sets can be tested and diagnosed down to the failing capacitor. To implement CODA a fixture mounted CMUX card must be fitted with one probe per device. Each CMUX card provides 32 channels, ample for most fixtures.

Production Line Integration

The 4250 series is designed to easily integrate into a high volume production line or to be used manually by an operator.

By selecting the horizontal interface model, in conjunction with the correct height setting, the 4250 series conforms to both SMEMA and de-facto European standards for manufacturing automation. A number of in-line handlers, from a variety of suppliers, have been integrated with the system, supported by the necessary communication protocols.

Specification

General Test Capabilities

Full in-circuit test (analog/digital/mixed signal)

Bus testing

Boundary Scan test

ISP (CPLD) device programming

Q-Test - Vectorless tests

Coda - Capacitor Polarity Tests

Analog functional card (Option)

System Controller

Pentium 4 PC

15 inch TFT Flat Screen monitor

Optional "Touch Screen"

PCI Bus

128 MBytes RAM

Windows 2000

IEEE-488 interface (option)

Serial ports (2 as standard, 2 optional)

Bar Code Reader (option)

Testpoint Count

128 - 2048 analog or universal test points

No multiplexing using FA23 test point cards

Multiplexing ratio of 4:1 using FA03 test point cards

128 testpoints per card

Analog Test Facilities

Contact test	*<100 kΩ*
Shorts test	*1 to 100 Ω*
Link test	*1 to 100 v*
Resistance DC	*0 Ω to 10 MΩ*
Resistance AC	*0 Ω to 1 MΩ*
Capacitance AC	*0 pF to 100 mF*
Capacitance DC	*1 µF to 100 mF*
Inductance	*0 H to 100 H*
Diode	*ON OFF*
Zener	*Voltage*
FET	*ON OFF RDS*
LED	*ON OFF*
Transformer	*Ratio 0.001 to 100*
Opto-isolator	
Transistor	*ON OFF HFE*

General Purpose Analog Facilities

DC stimulus (2 off)	*1 mV to 25 V*
	0 A to 100 mA
AC voltage stimulus	*0.1 V to 20 V pk-pk*
Frequency	*0.1 Hz to 20 kHz*
Noise	*<10 mV pk-pk 20 MHz b/w*
Waveshapes	*sine, square, triangle, ramp, up/down*
DC voltage measurement	*0 V to ±50 V*
DC current measurement	*0 A to ±100 mA*
AC voltage measurement	*0 V to 50 V*
Frequency measurement	*0.02 Hz to 5 MHz*
Period measurement	*10 µs to 65 s*
Programmable resistor	*0 Ω, 1 Ω to 10 MΩ in decade-steps*
Voltage limiter	

1149.1 Boundary-Scan Facilities (Option)

Any standard test pin may be used to perform Boundary-Scan tests. A configurable memory is accessible to all test pins providing the serial data needs for Boundary-Scan testing and permitting support for multiple scan paths.

Tests support:	*Integrity (Infrastructure) tests*
	Interconnection tests:
	Stuck & Open pins
	Shorts (Scan to scan)
	Shorts (Scan to test pin)

Digital Testing

Digital testing is full parallel drive, parallel sense.

Pattern rate	*5 MHz - multiple*
	Transitions per test step
Internal clock frequency	*50 MHz*
Clock divider	*1 to 256*
Test step period	*200 ns min with phase set movements*
Phase step period	*20 ns*
Timesets	*4*
Formats per time set	*6*
External clock	*50 MHz*
Phase lock	
Hardware Event	
Triggers	*4*
Phase lock multiplier	*1 to 16*
External sync	*up to 50 MHz*

Pattern generators (shift, rotate, increment) accessible to all pins

Flow control Instructions	*NOP, IF(NOT), CALL, RETURN, JUMP DELAY, LOOP, EXITLOOP, ENDLOOP, REPEAT, UNTIL, STOP, PAUSE*

Max Input Volt	-50 V to +50 V (logic relay open)
Control RAM depth	8 K
Flow trace RAM	64 K

FA03 Multiplexed Cards

Signature analysis (CRC)	per pin
Logic Families	1 per board
Drive high voltage range	-1.0 V to +14 V
Drive low voltage range	-6.0 V to +1.0 V
Sense levels	-8.0 V to +15 V
Drive high/low current	500 mA (forcing) 50 mA (non-forcing)
Slew rate	50 V/µs (slow) 150 V/µs (fast)
Backdrive timeout	10 µs to 650 ms
Relaxation timer	1 ms to 10 s
Testpin RAM depth	8 K
Pin face skew	20 ns
Digital Guarding	-2 static guards per TP board one high one low

FA23 non-Multiplexed Cards

Signature analysis (CRC)	per pin
Logic Families	1 per board
Drive high voltage range	+1.2 V to +5.4 V
Drive low voltage range	0 V to +1.5 V
Sense levels	0 V to +5.1 V
Drive high/low current	500 mA
Slew rate	60 V/µs
Backdrive timeout	10 µs to 650 ms
Relaxation timer	1 ms to 10 s
Testpin RAM depth	8 K per pin
Pin face skew	20 ns

Debug Facilities

Manual probe for in-circuit debug

Pin scan and search

Bug-probe

Busfail

UUT Power Supplies

Maximum of 6 supplies

2 types available:

0.15 V to 6.0 V, 25 A voltage and current programmable

1.0 V to 30.0 V, 7 A voltage and current programmable

Emergency Stop Button

System Software

MTL Test Language

High level, function based, structured programming language

Interactive edit and debug facilities

System self check

System self calibration

CAPG (Computer Assisted Program Generator) Option

32 bit Windows application

Generic device library

CAD (.cb file) or manual input

Supports 42xx, 52xx and 53xx series

Safe check digital back-driving analysis software

Extensions for bus testing

ISP device programming

Boundary-Scan test generation (Option)

Multi-board (option)

FABmaster CAD Interface (Option)

i-Base5 Information Management System (Option)

Migration Software Tools

Options for:

IFR/Marconi System 80 series
Agilent/HP307x series
Philips ICCT2000
GenRad 227x/228x

Operating Conditions

Mains supply	90 to 264 volts, 47 Hz to 63 Hz, single phase 13 A
Power consumption	2 kVA
Operating temp range	+10°C to +35°C
Humidity range	25% RH to 75% RH

Dimensions (Approx)

4250 Flat Interface model:

Height	Depth	Width
800 mm	940mm	1180mm

4250 inclined (60°) interface model:

Height	Depth	Width
1230 mm	940mm	1180mm

Weight

227 kg

Vacuum Actuation

-20 in Hg (-0.66 Bar) to -28 in Hg (-0.94 Bar)

Fixturing

Vacuum operated interface

System interface life	≥30,000 operations
Fixture to interface life	≥5,000 operations

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